introducing a first impurity imparting n-type into said first low concentration n-type impurity region and said second low concentration n-type impurity region and said third low concentration n-type impurity region;

forming a first photoresist and a second photoresist and a third photresist respectively over said first semiconductor island and said second semiconductor island and said third semiconductor island so that said first photoresist partially overlaps with said first low concentration n-type impurity region and said second photoresist partially overlaps with said second low concentration n-type impurity region and said third photoresist partially overlaps with said third low concentration n-type impurity region;

forming a first high concentration n-type impurity region and a second high concentration n-type impurity region and a third high concentration n-type impurity region respectively in said first semiconductor island and said second semiconductor island and said third semiconductor island by introducing a second impurity imparting n-type into a first part of each of said first low concentration n-type impurity region and said second low concentration n-type impurity region and said third low concentration n-type impurity region using said first photoresist and said second photoresist and said third photoresist as masks to leave behind second parts provided under said masks in said first low concentration n-type impurity region and said second low concentration n-type impurity region and said third low concentration n-type impurity region as they are; and

introducing impurities imparting p-type into said second low concentration n-type impurity region and said second high concentration n-type impurity region to change said second low concentration n-type impurity region and said second high concentration n-type impurity region to a p-type impurity region,

wherein concentration of said second impurity is higher than concentration of said first impurity,

wherein said first semiconductor island is formed in an n-channel thin film transistor of a driving circuit,

wherein said second semiconductor island is formed in a p-channel thin film transistor of said driving circuit, and

wherein said third semiconductor island is formed in a pixel thin film transistor.

30 (Twice Amended). A method according to claim 64, wherein, said p-type impurity region is formed in said p channel thin film transistor of said driving circuit in a selected region of said second semiconductor island after said step of forming said protective insulation film comprising an inorganic insulating material, over a gate electrode of said p channel thin film transistor, and an offset region is formed between a channel formation region of said p channel thin film transistor and said p type impurity region.

Cancel Claims 32, 33 and 53.

54 (Amended). A method according to claim 64 wherein said protective insulation film comprises a material selected from the group consisting of silicon oxide, silicon oxide nitride and silicon nitride.

55 (Amended). A method according to claim 64 wherein said protective insulation film has a thickness of 100 to 200 nm.

56 (Amended). A method according to claim 64 wherein said inter-layer insulation film has a mean thickness of 1.0 to 2.0 μm.

57 (Amended). A method according to claim 64 wherein said inter-layer insulation film comprises a material selected from the group consisting of polyimide, acryl, polyamide, polyimidamide and benzocyclobutene.

58 (Amended). A method according to claim 64 wherein said pixel electrode comprises a Ti film and an Al film.

59 (Amended). A method according to claim 29 wherein said p channel thin film transistor has a single drain structure.

60 (Amended). A method according to claim 29 wherein said first low concentration n-type impurity region of said first semiconductor island formed in said n channel thin film transistor of said driving circuit have a length of 1.0 to 4.0 μm.

61 (Amended). A method according to claim 29 wherein said third low concentration n-type impurity region of said third semiconductor island formed in said pixel thin film transistor have a length of 0.5 to 4.0 μm.

62 (Amended). A method according to claim 29 wherein said first and second and third semiconductor islands have a thickness of 25 to 80 μm.